IDEC Chip Design Contest

A 0.5V-V_{IN}, 0.29ps-Transient-FOM, and Sub-2mV-Accuracy Adaptive-Sampling Digital LDO Using Single-VCO-Based Edge-Racing Time Quantizer

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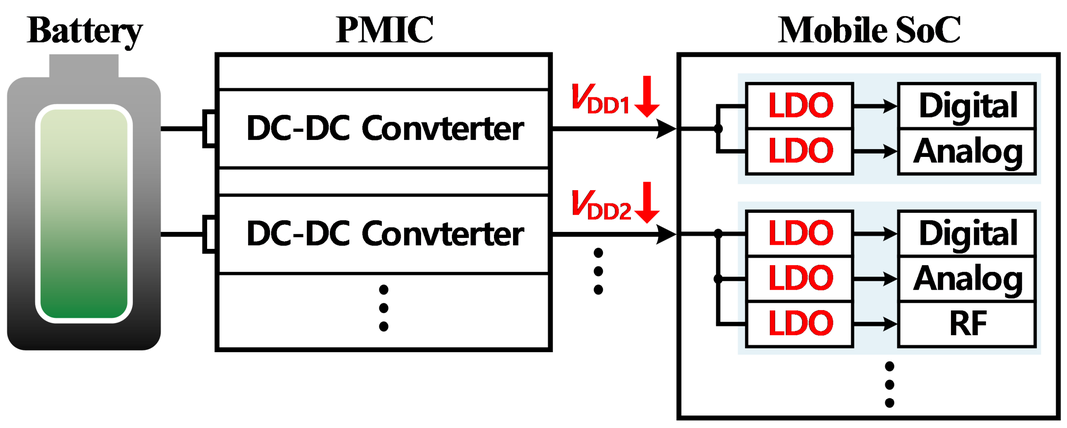
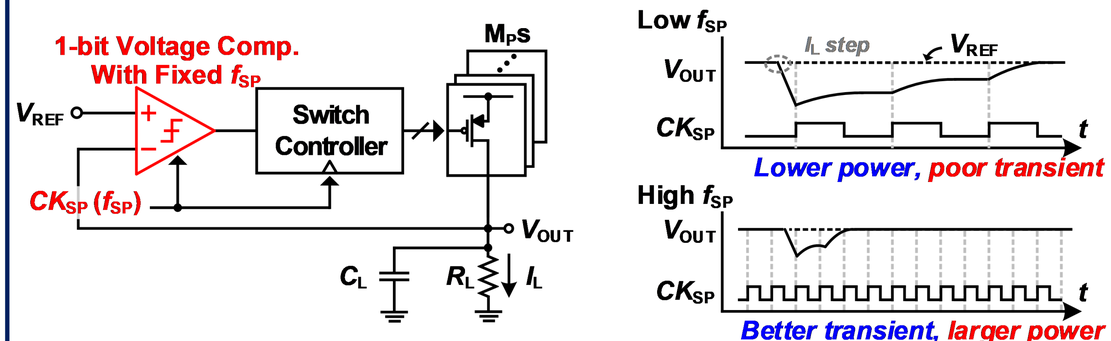
Motivation



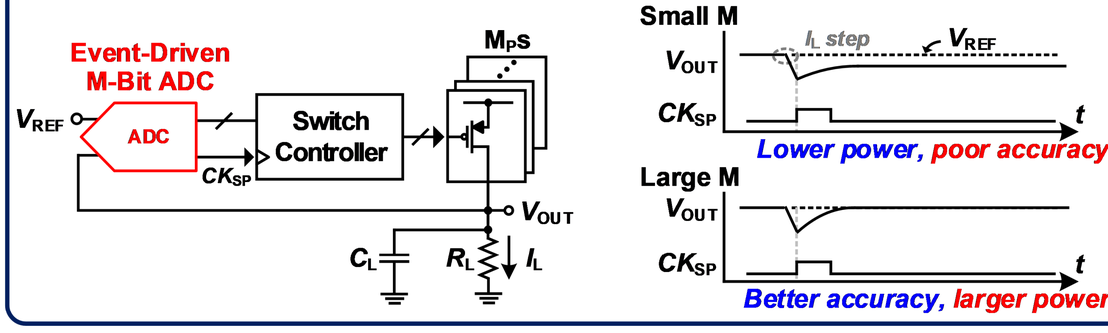
- DC-DC converter providing supply voltages w/ high efficiency
- LDO regulating the supply voltages to optimal levels
- Dynamic V_{DD}-scaling, popular to save power
  – Needs of providing ultra-low V_{DD}s in an efficient way
- Demanding reliable operation of LDOs under ultra-low V_{DD}

Problems of Prior Architectures

Digital LDO Using Voltage Comparator [3]: Trade-off btw Power & Transient

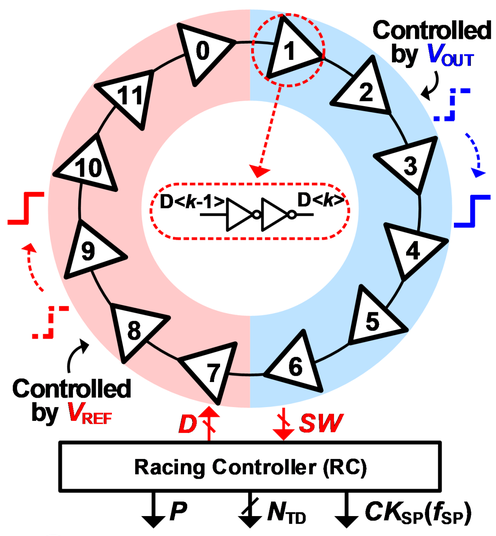


Digital LDO Using Multi-bit ADC [2]: Trade-off btw Power & Accuracy



Concept of Proposed Idea

Single-VCO-Based Edge-Racing(SVER) Time Quantizer

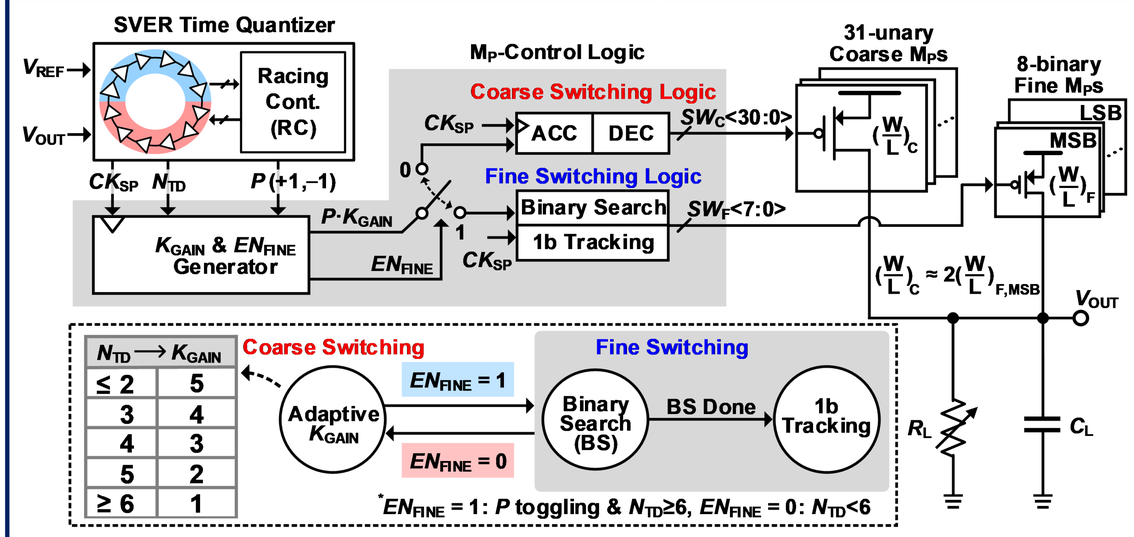


Operation

- Two rising edges equally passing through all delay cells
- Traveling speed of the two rising edges are determined by different control voltages, V_{OUT} & V_{REF}
- Race stops and decision made, when the distance between two edges reduced

☺ High accuracy w/o mismatches btw delay cells
☺ Magnitude and polarity of voltage difference
☺ Very high maximum f_{SP} available ➔ $max(f_{SP}) = N/2 * max(f_{REF}, f_{OUT})$

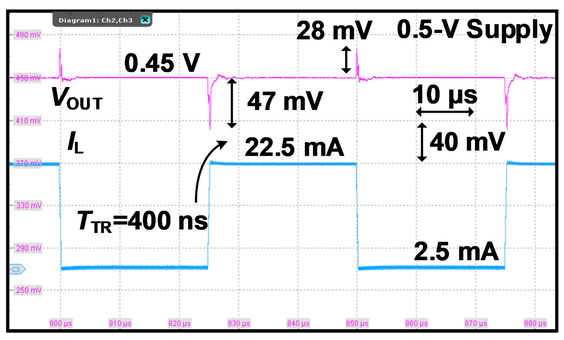
Architecture of Proposed DLDO

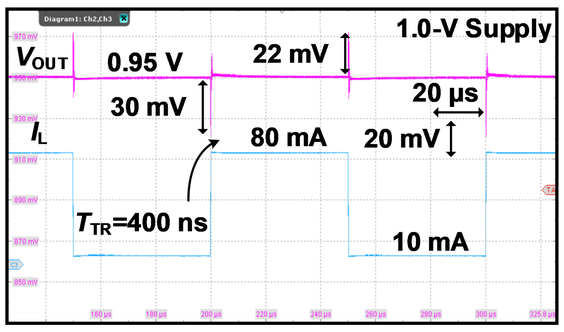


- SVER time quantizer compares V_{OUT} with V_{REF}, and delivers the information of the racing result to the MP-Control Logic
- The MP-Control Logic controls the switches of the coarse and the fine pass transistors

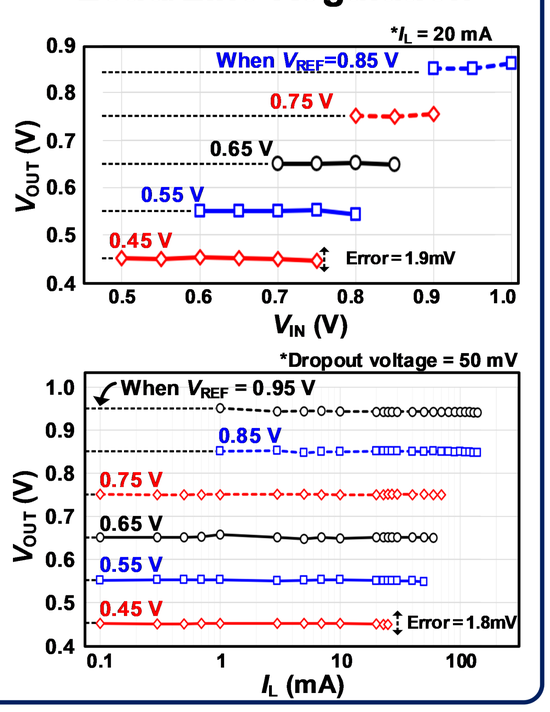
Measurement Transient & Regulation

Load Transient Response





Load/Line Regulation

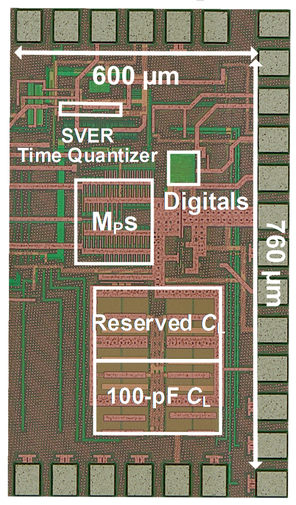


Performance Comparison

	This work	ISSCC18[1]	ISSCC17[2]	ISSCC17[3]	ISSCC16[4]
Process	65 nm	65 nm	65 nm	65 nm	28 nm
Quantizer type	SVER	Replica VCO	Multi-bit ADC	1-bit Compar.	Multi-bit ADC
V_{IN} (V)	0.5 – 1.0	0.6 – 1.2	0.45 – 1.0	0.5 – 1.0	1.1
V_{OUT} (V)	0.45 – 0.95	0.4 – 1.1	0.4 – 0.95	0.3 – 0.45	0.9
$I_{L,MAX}$ (mA)	25	100	3.356	2	200
C_L (nF)	0.1	0.04	0.1	0.4	23.5
T_{SETTLE} (µs)	1.2	1.24	1.41	0.1	20
Quiescent I_Q (µA)	25 – 127	100 – 1070	8.1 – 258	14	NA
ΔV_{OUT} (mV) @ΔI_L (mA)	47 @ 20	108 @ 50	34 @ 1.44	40 @ 1.06	120 @ 180
**FOM_{TR} (ps)	0.29	1.38	20	199.4	9.6
Load regulation (mV/mA)	0.072	0.72*	2.5*	< 5.6	NA
Area (mm^2)	0.0488	0.0374	0.03	0.0023	0.021

*Estimated from measurement results
**FOM_{TR}: $C_L \cdot \Delta V_{OUT} \cdot I_Q / \Delta I_L^2$

Die Micrograph



The smallest transient FOM and the best load regulation, while it used 0.5-V supply. And it had a small ΔV_{OUT} by using SVER time quantizer

References
[1] S. Kundu *et al.*, *ISSCC*, pp. 308-310, Feb. 2018 [2] D. Kim *et al.*, *ISSCC*, pp. 148-149, Feb. 2017. [3] L. Salem, *et al.*, *ISSCC*, pp. 340–341, Feb. 2017. [4] Y. Lee *et al.*, *ISSCC*, pp. 150-151, Feb. 2016.

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